IPC-16A/520D MOS/LSI single chip 16-bit microprocessor (PACE)

user benefits

- Simplified programming
- Simplified I/O design
- Simplified system configurations
- Simplified prototyping

PACE features

- 45 instruction types
- All instruction single-word
- Multiple addressing modes
  - Program-counter relative
  - Base page
  - Indexed
  - Direct and indirect
- Four general-purpose accumulators
- Byte and word processing
- Common memory and peripheral addressing
- Six hardware-vectored priority interrupts
- 10-word on-chip stack
- Four control flag outputs
- Three sense inputs
- Four I/O control strobe signals
- CPU in single 40-pin package supported by single-chip
  - Timing element
  - Transceivers
  - Address latches
  - I/O ports
  - 1k x 16 ROM
- Chip kits
- Application cards
- Development systems
- Full array of software
  - Assemblers
  - Cross assemblers
  - Loaders
  - Editor
  - Debug
  - Diagnostics

block diagram

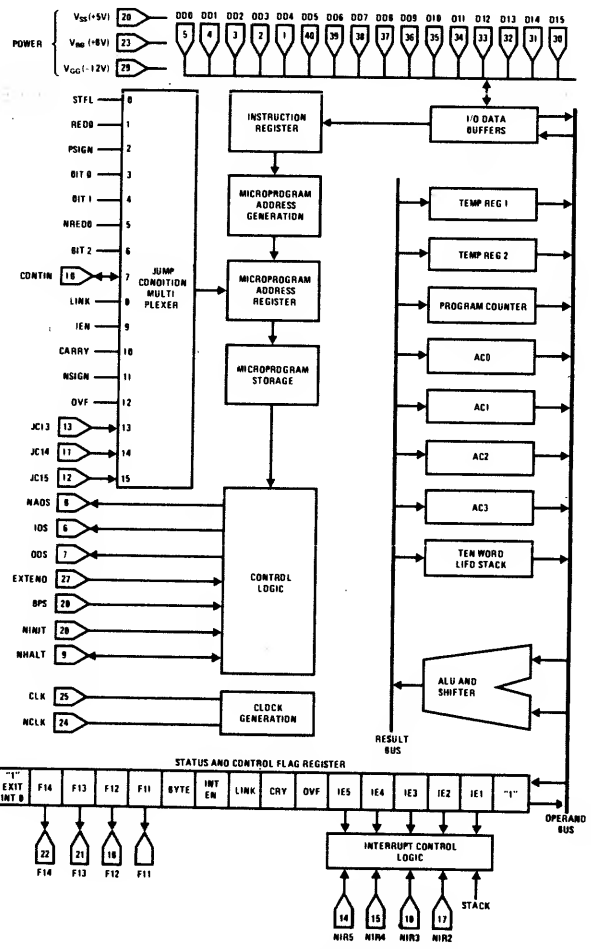

FIGURE 1. PACE Detailed Block Diagram

general description and functional highlights

PACE (Processing and Control Element) is a single-chip, 16-bit microprocessor packaged in a standard, hermetically sealed, 40-pin ceramic dual-in-line package. PACE utilizes silicon gate enhancement mode process technology which ensures high performance, high reliability and high producibility.

PACE is intended for use in applications where the convenience and efficiency of 16-bit word length is desired while maintaining the low cost inherent in single-chip, fixed instruction microprocessors. PACE is a true 16-bit central processor unit: it makes use of 16-bit instruction words and 16-bit data words, and features a powerful, efficient, and flexible set of 45 instructions. All instructions use a single-word, 16-bit format thus reducing memory accesses and program storage requirements. A unique feature of PACE is the ability to operate on both 8- and 16-bit data words: this extends the inherent efficiency and power of a 16-bit processor to 8-bit applications.

The architecture of PACE (shown in *Figure 1*) features a number of resources to minimize system program and read/write storage, increase throughput, and reduce the amount and cost of external support hardware. The principal resources that allow these efficiencies to be achieved include:

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FOUR 16-BIT GENERAL PURPOSE WORKING REGISTERS available to the user reduce the number of memory load and store operations associated with saving temporary and intermediate results in system memory.

AN INDEPENDENT 16-BIT STATUS AND CONTROL FLAG REGISTER automatically and continuously preserves system status. The user may operate on its contents as data, allowing masking, testing and modification of several bit fields simultaneously.

A TEN WORD (16-BIT) LAST-IN, FIRST-OUT (LIFO) STACK inherently decreases response time to interrupts while eliminating both program and read/write system storage overhead associated with storing stack information outside the microprocessor chip.

STACK FULL/STACK EMPTY interrupts are provided to facilitate off-chip stack storage in those applications where additional stack capacity is desirable.

A SIX LEVEL, VECTORED PRIORITY INTERRUPT SYSTEM internal to the chip provides automatic interrupt identification, eliminating both program storage overhead and the time normally required to poll peripherals in order to identify the interrupting device.

THREE SENSE INPUTS AND FOUR CONTROL FLAG OUTPUTS allow the user to respond directly to specific combinations of status present in the microprocessor-based system, thus eliminating costly hardware, program overhead and throughput associated with implementing these functions over the system data bus.

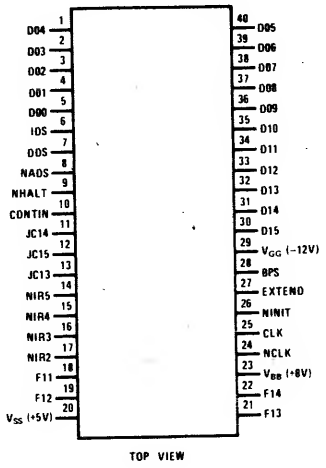
A COMPREHENSIVE SET OF INPUT/OUTPUT CONTROL SIGNALS provided by the internal Control Logic simplifies interfaces to memory and peripherals and allows flexible control of PACE operations.

SINGLE-PHASE TRUE AND COMPLEMENT CLOCK INPUTS are easily generated with a minimum of external components.

PACE interface signal descriptions

The functions of each of the PACE signals are described below. Timing specifications for the signals are provided in the table of electrical characteristics and associated diagrams. Pin assignments are shown in *Figure 2*.

Dual-In-Line Package



TOP VIEW

FIGURE 2. PACE Pin Assignments

CLK, NCLK (inputs) – External true and complemented clock inputs.

D00-D15 (input/output) – Data bus lines. Bidirectional MOS data lines used for input and output of data and for output of 16-bit addresses on I/O cycles.

NADS (output) – Address Data Strobe. The negative-true NADS signal is sent out at the beginning of every data input/output cycle and indicates that a memory or peripheral address has been output on the data bus lines. The address is stable on the data bus while the NADS signal is active low.

ODS (output) – Output Data Strobe. The ODS signal indicates to external circuits that the data bus contains valid output data.

IDS (output) – Input Data Strobe. The IDS signal indicates to external devices that PACE is performing a data input cycle. The signal should be used by memory or peripheral devices to gate data onto the PACE data bus lines.

EXTEND (input) – Extended Data Transfer. The EXTEND signal is used by slower memory or peripheral devices to temporarily increase time duration of data input/output transfers. The EXTEND signal should be driven high at the beginning of ODS or IDS signal and held high until output data has been captured or input data is made available to data bus. The EXTEND signal can also be used to suspend input/output operations by applying the signal after the end of ODS or IDS.

JC13, JC14, JC15 (input) – Jump Conditions 13, 14, and 15. JC13, 14, and 15 are user-specified inputs that can be tested using Branch-On-Condition (BOC) Instructions. If jump condition input specified in BOC Instruction is high, a program branch is effected. The JC13-JC15 signals are useful for testing status of external devices and receiving serial data.

F11, F12, F13, F14 (output) – General-purpose control flag outputs from PACE Status and Control Flags Register. Individual flags may be set by Set Flag Instruction and pulsed or reset by Pulse Flag Instruction. The F11-F14 signals may be used for direct control of system functions or serial data output.

NIR2, NIR3, NIR4, NIR5 (input) – Interrupt Requests 2, 3, 4, and 5. When these negative-true input signals are low for 1 CLK period, minimum, the associated internal Interrupt Request Latch is set if the corresponding interrupt enable has been set by users program. The interrupt will be serviced after completion of current instruction if the Master Interrupt Enable is set. Interrupt Requests are prioritized, with NIR5 having lowest priority.

NHALT (input/output) – Halt. When the negative-true NHALT signal is driven low by external logic, it effects microprocessor stall or Level-0 Interrupt, depending on timing of CONTIN signal. When not controlled by external logic, NHALT is driven low by PACE for 7/8 duty cycle while programmed halt condition exists. Programmed halt is initiated by the Halt Instruction and terminated by pulsing CONTIN line via external logic.

CONTIN (input/output) – Continue. The CONTIN signal is used in input mode to terminate programmed halt, or to exercise microprocessor stall and Level-0 Interrupt, or as a jump-condition input that can be tested using a BOC instruction. In the output mode, CONTIN transmits an interrupt acknowledge pulse to acknowledge CPU response to an active interrupt input.

BPS (input) – Base Page Select. The BPS signal enables one of two base-page addressing schemes to be selected. When BPS is low, first 256 words of memory constitute base page (page zero). When BPS is high, first 128 memory words and last 128 memory words constitute base page.

NINIT (input) – Initialize. While the negative-true NINIT signal is low, PACE operation is suspended, and IDS/ODS signals are set to inactive state. After NINIT completes low-to-high transition, the program counter is set to zero, the internal stack pointer is cleared, and all flags and interrupt enables are set low except Level-0 Interrupt Enable which is set high. All other registers contain arbitary values.

V_{SS}	+5 Volts
V_{GG}	−12 Volts
V_{BB}	V_{SS} +3 Volts (substrate bias)

interrupt system

The PACE microprocessor provides a six level, vectored, priority interrupt structure. This allows automatic identification of an interrupting device's level and allows all devices on an interrupt level to be enabled or disabled as a group, independent of other interrupt levels. An individual interrupt enable is provided in the status register for each level, as shown in *Figure 3*, and a master interrupt enable (IEN) is provided for all 5 lower priority levels as a group. Negative true interrupt request inputs are provided to allow several interrupts to be "wire-ORed" on each input. When an interrupt request occurs, it will set the interrupt request latch if the corresponding interrupt enable is true. The latch will be set by any pulse exceeding one clock period in duration, which is useful for capturing narrow timing or control pulses. If the master interrupt enable (IEN) is true, then an interrupt will be generated. During the interrupt sequence an address is provided by the output of the priority encoder and is used to access the pointer for the highest-priority interrupt request (IR0 is highest priority, IR5 is lowest priority). The pointers are stored in locations 2–7 (see Table 1) for interrupt requests 1–5 and 0, respectively. The pointer specifies the starting address of the interrupt service routine for that particular interrupt level. Before executing the

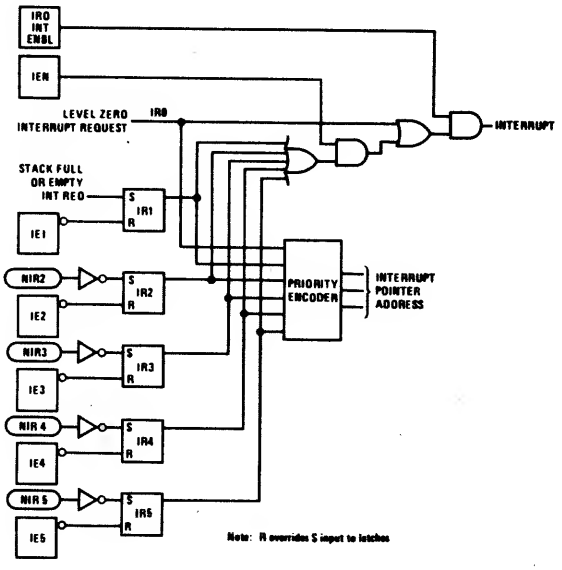


FIGURE 3. Interrupt System

interrupt service routine, the program counter is pushed on the stack and IEN is set false. The interrupt service routine may set IEN true after turning off the interrupt enable for the level currently being serviced (or resetting the interrupt request). (The interrupt enables may be set and reset using the SFLG and PFLG instructions.)

TABLE 1. Interrupt Pointer Table

8	Int 0 Program
7	Int 0 PC Pointer
6	Int 5 Pointer
5	Int 4 Pointer
4	Int 3 Pointer
3	Int 2 Pointer
2	Int 1 Pointer
1	Not Assigned
Loc 0	Initialization Inst

The non-maskable level zero interrupt (IR0) is an exception to this interrupt procedure. It has a program counter storage location pointer (the program counter is not stored on the stack for this particular interrupt in order to preserve the processor state) which is followed by the level zero interrupt service routine. The IR0 interrupt enable is cleared when a level zero interrupt occurs (IEN is unaffected) and may be set true by setting (non-existent) status flag 15. This allows execution of one more instruction (typically JMP@) to return from the IR0 interrupt routine before another interrupt will be acknowledged. This interrupt level is typically used by the control panel, which then can always interrupt the application program and does not affect system status. Level zero interrupts are generated by exercising the NHALT and CONTIN lines.

instruction summary

The instruction set is divided into eight instruction classes as listed in Table 3. The branch instructions provide the means to transfer control anywhere in the 16-bit addressing space. Conditional branches are effected using the BOC instruction, which allows testing any one of 16 conditions, including status flags, the contents of AC0, and user inputs to the chip. Additional testing capability is provided by the skip instructions, which provide memory or peripheral to register comparisons without altering data. The memory data transfer instructions provide data transfers between the accumulators and memory or peripheral devices. The load with sign extended is provided to convert 8-bit, two's complement data to 16-bit data, allowing 16-bit address modification when the 8-bit data length has been selected.

The memory data operate instructions provide operations between the principal working register (AC0) and memory or peripheral data. This includes both binary and BCD arithmetic instructions. The register data transfer instructions provide a very complete set of transfer possibilities between the accumulators, flag register and stack, and include the capability to load immediate data. Register data operate instructions provice logical and arithmetic operations between any two accumulators. They may be used for address and data modification and to reduce the number of (time consuming) memory references in a program. The shift and rotate instructions allow 8 different operations which are useful for multiply, divide, bit scanning and serial input-output operations. The miscellaneous instructions include the capability to set or reset (pulse) any of the 16 bits of the status flag register individually.

The power of the instruction set is further enhanced by a flexible memory addressing scheme that provides three floating memory pages and one fixed page of 256 words each. Instructions which use both direct and indirect memory addressing are included in the instruction set. Three modes of direct memory addressing are available: base page, program counter relative, and index register relative. The mode of addressing is specified by the XR field of the instruction shown in the "Instruction Format" column of Table 3. Table 2 summarizes the direct addressing modes available.

TABLE 2. Direct Addressing Modes

XR Field	Addressing Mode	Effective Address
00	Base Page	EA = disp
01	Program Counter Relative	EA = disp + (PC)
10	AC2 Relative (indexed)	EA = disp + (AC2)
11	AC3 Relative (indexed)	EA = disp + (AC3)

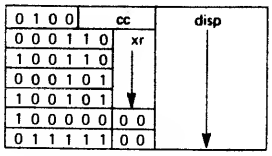
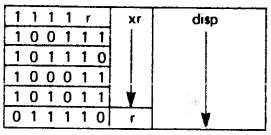
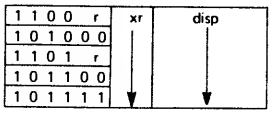
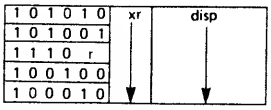
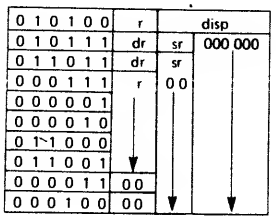
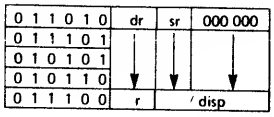
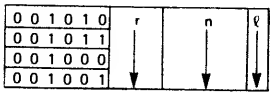
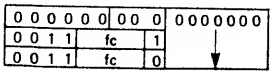
Note 1: For base page addressing, disp is positive and in the range of 000 to 255 if BPS = 0, and is a signed number in the range of −128 to +127 if BPS = 1.
Note 2: For relative addressing, disp has a range of −128 to +127.

Indirect addressing consists of first establishing an address in the same fashion as with direct addressing [by either the base page, relative to PC, or indexed (relative to AC2 or AC3) mode]. The 16-bit contents of the memory location at this address is then used as the address of the operand, allowing any memory location to be addressed.

drivers and receivers

Equivalent circuits for PACE drivers and receivers are shown in *Figure 4*. All inputs have static charge protection circuits consisting of an RC filter and voltage clamp. These devices should still be handled with care, as the protection circuits can be destroyed by excessive static charge. Pullup transistors on several inputs are turned on during one of the eight internal clock phases. In the case of bidirectional signals, the output driver transistors also serve as input pullup transistors.

TABLE 3. PACE Instruction Summary

Mnemonic	Meaning	Operation	Maximum Execution Time (Note)	Instruction Format
1. Branch Instructions				
BOC	Branch On Condition (Table 4)	(PC) ← (PC) + disp if cc true	$5M + E_R + 1M$ if branch	
JMP	Jump	(PC) ← EA	$4M + E_R$	
JMP@	Jump Indirect	(PC) ← (EA)	$4M + 2E_R$	
JSR	Jump To Subroutine	(STK) ← (PC), (PC) ← EA	$5M + E_R$	
JSR@	Jump To Subroutine Indirect	(STK) ← (PC), (PC) ← (EA)	$5M + 2E_R$	
RTS	Return from Subroutine	(PC) ← (STK) + disp	$5M + E_R$	
RTI	Return from Interrupt	(PC) ← (STK) + disp, IEN = 1	$6M + E_R$	
2. Skip Instructions				
SKNE	Skip if Not Equal	If (ACr) ≠ (EA), (PC) ← (PC) + 1	$5M + 2E_R + 1M$ if skip	
SKG	Skip if Greater	If (AC0) > (EA), (PC) ← (PC) + 1	$7M + 2E_R + 1M$ if skip	
SKAZ	Skip if And is Zero	If [(AC0) ∧ (EA)] = 0, (PC) ← (PC) + 1	$5M + 2E_R + 1M$ if skip	
ISZ	Increment and Skip if Zero	(EA) ← (EA) + 1, if (EA) = 0, (PC) ← (PC) + 1	$7M + 2E_R + E_W + 1M$ if skip	
DSZ	Decrement and Skip if Zero	(EA) ← (EA) − 1, if (EA) = 0, (PC) ← (PC) + 1	$7M + 2E_R + E_W + 1M$ if skip	
AISZ	Add Immediate, Skip if Zero	(ACr) ← (ACr) + disp, if (ACr) = 0, (PC) ← (PC) + 1	$5M + E_R + 1M$ if skip	
3. Memory Data Transfer Instructions				
LD	Load	(ACr) ← (EA)	$4M + 2E_R$	
LD@	Load Indirect	(AC0) ← ((EA))	$5M + 3E_R$	
ST	Store	(EA) ← (ACr)	$4M + E_R + E_W$	
ST@	Store Indirect	((EA)) ← (AC0)	$4M + 2E_R + E_W$	
LSEX	Load With Sign Extended	(AC0) ← (EA) bit 7 extended	$4M + 2E_R$	
4. Memory Data Operate Instructions				
AND	And	(AC0) ← (AC0) ∧ (EA)	$4M + 2E_R$	
OR	Or	(AC0) ← (AC0) ∨ (EA)	$4M + 2E_R$	
ADD	Add	(ACr) ← (ACr) + (EA), OV, CY	$4M + 2E_R$	
SUBB	Subtract with Borrow	(AC0) ← (AC0) + ~ (EA) + (CY), OV, CY	$4M + 2E_R$	
DECA	Decimal Add	(AC0) ← (AC0) $+_{10}$ (EA) $+_{10}$ (CY), OV, CY	$7M + 2E_R$	
5. Register Data Transfer Instructions				
LI	Load Immediate	(ACr) ← disp		
RCPY	Register Copy	(ACdr) ← (ACsr)	$4M + E_R$	
RXCH	Register Exchange	(ACdr) ← (ACsr), (ACsr) ← (ACdr)	$4M + E_R$	
XCHRS	Exchange Register and Stack	(STK) ← (ACr), (ACr) ← (STK)	$6M + E_R$	
CFR	Copy Flags Into Register	(ACr) ← (FR)	$6M + E_R$	
CRF	Copy Register Into Flags	(FR) ← (ACr)	$4M + E_R$	
PUSH	Push Register Onto Stack	(STK) ← (ACr)	$4M + E_R$	
PULL	Pull Stack Into Register	(ACr) ← (STK)	$4M + E_R$	
PUSHF	Push Flags Onto Stack	(STK) ← (FR)	$4M + E_R$	
PULLF	Pull Stack Into Flags	(FR) ← (STK)	$4M + E_R$	
			$4M + E_R$	
6. Register Data Operate Instructions				
RADD	Register Add	(ACdr) ← (ACdr) + (ACsr), OV, CY		
RADC	Register Add With Carry	(ACdr) ← (ACdr) + (ACsr) + (CY), OV, CY		
RAND	Register And	(ACdr) ← (ACdr) ∧ (ACsr)	$4M + E_R$	
RXOR	Register Exclusive OR	(ACdr) ← (ACdr) ∀ (ACsr)	$4M + E_R$	
CAI	Complement and Add Immediate	(ACr) ← ~ (ACr) + disp	$4M + E_R$	
			$4M + E_R$	
			$5M + E_R$	
7. Shift And Rotate Instructions				
SHL	Shift Left	(ACr) ← (ACr) shifted left n places, w/wo link	$(5 + 3n)\ M + E_R$, n = 1 − 127; $6M + E_R$, n = 0	
SHR	Shift Right	(ACr) ← (ACr) shifted right n places, w/wo link		
ROL	Rotate Left	(ACr) ← (ACr) rotated left n places, w/wo link		
ROR	Rotate Right	(ACr) ← (ACr) rotated right n places, w/wo link		
8. Miscellaneous Instructions				
HALT	Halt	Halt		
SFLG	Set Flag (Table 5)	(FR) $_{fc}$ ← 1	$5M + E_R$	
PFLG	Pulse Flag (Table 5)	(FR) $_{fc}$ ← 1, (FR) $_{fc}$ ← 0	$6M + E_R$	

Note: M = Machine cycle time = 4 clock periods
n = number of shifts
E_R = Extend time for read cycle
E_W = Extend time for write cycle
External interrupt response time is $7M + E_R$ plus time to finish current instruction.

TABLE 4. Branch Conditions

Number	Mnemonic	Condition
0	STFL	Stack full
1	REQ0	(AC0) equal to zero(1)
2	PSIGN	(AC0) has positive sign(2)
3	BIT 0	Bit 0 of AC0 true
4	BIT 1	Bit 1 of AC0 true
5	NREQ0	(AC0) is non-zero(1)
6	BIT 2	Bit 2 AC0 is true
7	CONTIN	CONTIN (continue) input is true
8	LINK	LINK is true
9	IEN	IEN is true
10	CARRY	CARRY is true
11	NSIGN	(AC0) has negative sign(2)
12	OVF	OVF is true
13	JC13	JC13 input is true
14	JC14	JC14 input is true
15	JC15	JC15 input is true

Note 1: If the selected data length is 8 bits, only bits 0-7 of AC0 are tested.
Note 2: Bit 7 is the sign bit (instead of bit 15) if the selected data length is 8 bits.

TABLE 5. Status and Control Flags

Register Bit	Flag Name	Function
0	"1"	Not used—always logic 1
1	IE1	Interrupt Enable Level 1
2	IE2	Interrupt Enable Level 2
3	IE3	Interrupt Enable Level 3
4	IE4	Interrupt Enable Level 4
5	IE5	Interrupt Enable Level 5
6	OVF	Overflow
7	CRY	Carry
8	LINK	Link
9	IEN	Master Interrupt Enable
10	BYTE	8-bit data length
11	F11	Flag 11
12	F12	Flag 12
13	F13	Flag 13
14	F14	Flag 14
15	"1"	Always logic 1, set for Interrupt 0 exit

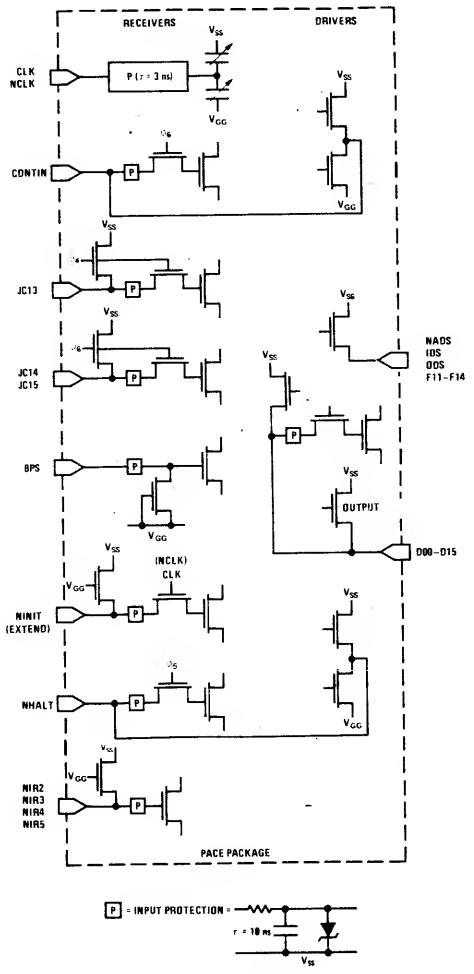
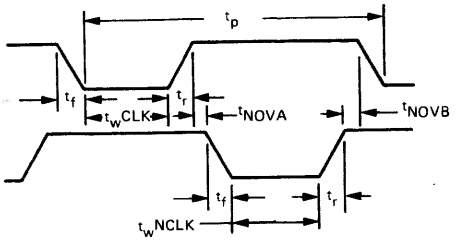


FIGURE 4. PACE Driver and Receiver Equivalent Circuits

external clock timing

PACE requires non-overlapping true and complemented clock inputs as shown in *Figure 5*. Refer to Electrical Characteristics for timing specifications.



where:
t_p = CLOCK PERIOD
$t_{NOVA} = t_{NOVB}$ = CLOCK NONOVERLAP
$t_{WCLK} = t_{WNCLK}$ = CLOCK WIDTH

FIGURE 5. External Clock Timing

initialization

The PACE control circuitry may be initialized at any time by use of the NINIT input signal. The effects of the NINIT signal are described under "PACE Signal Descriptions." The NINIT signal should always be used to initialize the processor after applying power. The minimum pulse width for NINIT is 8 clock periods (see *Figure 6*). The PACE data strobes (NADS, ODS, IDS) are inactive for 16 clock periods after the trailing edge of the NINIT Signal. After the 16 clock periods, the first NADS signal occurs and the first instruction is accessed from memory location zero.

Note: If the NINIT signal is held low while clocks and/or power are first being applied, the NADS and NHALT outputs may have an undefined state for 8 clock periods after the trailing edge of NINIT.

data input/output operations

All data transfers between PACE and external memories or peripheral devices take place over the 16 data lines. These transfers are synchronized by the NADS, IDS, ODS and EXTEND signals. Timing for address data output is shown in *Figure 7*. Where signal timing is referenced to clocks, the reference is to valid logic "1" or logic "0" clock levels. Cross-hatched areas indicate uncertainty of output transitions or "don't care" (optional) states for data inputs. Address data becomes valid one clock phase prior to the Address Data Strobe (NADS) and remains valid for one clock phase afterwards. Typically, NADS will be used to strobe the address data into a latch, either internal or external to the memory chips, or to clock decoded peripheral addresses into a flip-flop.

The PACE address output drivers assume a high impedance state during the data input interval as shown in *Figure 7*. The IDS signal may be used to disable the output sense amplifiers and enable TRI-STATE® input buffers. Increased power supply current may occur during the transition period of the TRI-STATE enable signal, when several devices may be simultaneously enabled. Therefore, good power and ground layout and bypass filtering practice should be observed. The data lines must be driven to valid input data logic levels by the end of IDS. TTL devices will actively drive the input to an intermediate level of $V_{SS} - 2.35V$ and the transition will be completed by a combination of the on-chip pullup transistor and the (reduced) TTL output drive current. Typically, this data input timing will allow operation of the microprocessor in a system at maximum speed if the access time of the system memory is less than 2 clock periods. For memories with longer access times the clock frequency may be reduced or the I/O cycle extend feature may be used, as described below.

Data output timing is shown in *Figure 8*. Output data becomes valid at the leading edge of ODS and remains valid for one clock period following the trailing edge. The Output Data Strobe is typically used as a read-write signal for memory and an output data latch strobe for peripheral interfaces.

For systems utilizing memories with access times greater than 2 clock periods it may be desirable to use the EXTEND input to lengthen the I/O cycle by multiples of the clock period. Timing for this is shown in *Figure 9*. In the case of either input or output operations, the extend should be brought true prior to the end of internal phase 6. The timing shown in *Figure 9* will provide the minimum extend of one clock period. Holding EXTEND true for n additional clock periods longer will cause an extension of n + 1 clock periods.

In DMA or multiprocessor systems it may be desirable to prevent I/O operations by PACE when the bus is in use by another device. This may be done by using the EXTEND signal immediately following an IDS or ODS as shown in *Figure 10*. Alternatively, the extend timing of *Figure 9* may be used, as the extend function occurs independent of whether there is an I/O operation, that is, whenever the internal clock phase 6 occurs.

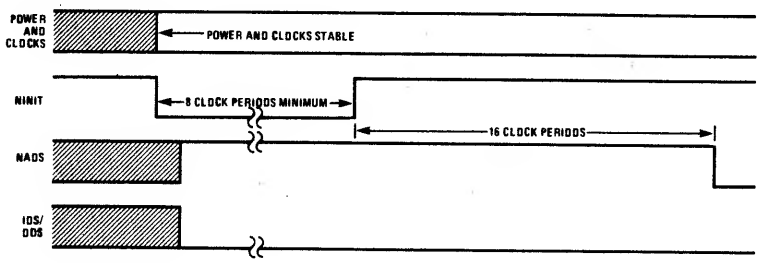


FIGURE 6. Initialization Timing

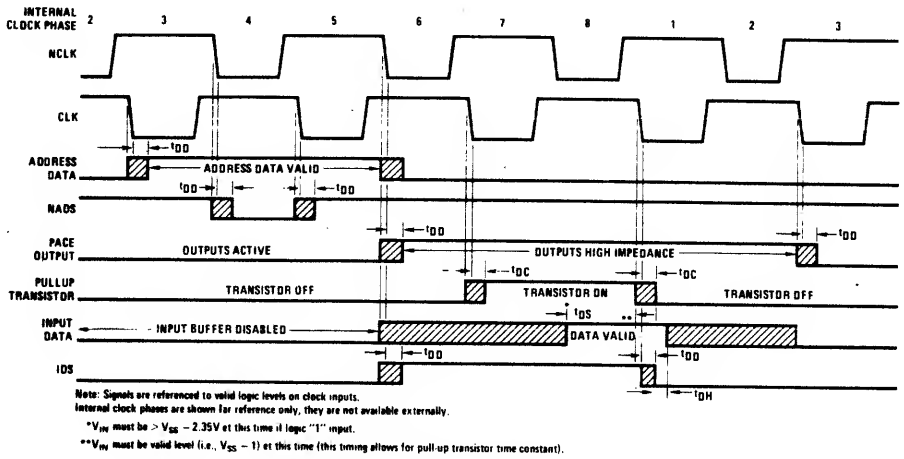


Figure 7. Address Output and Data Input Timing

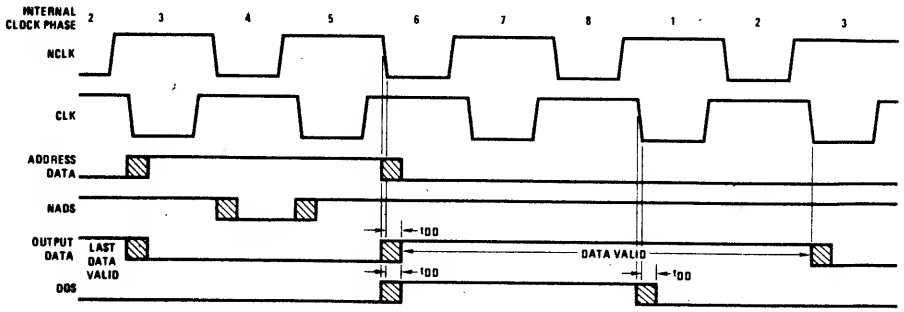


FIGURE 8. Data Output Timing

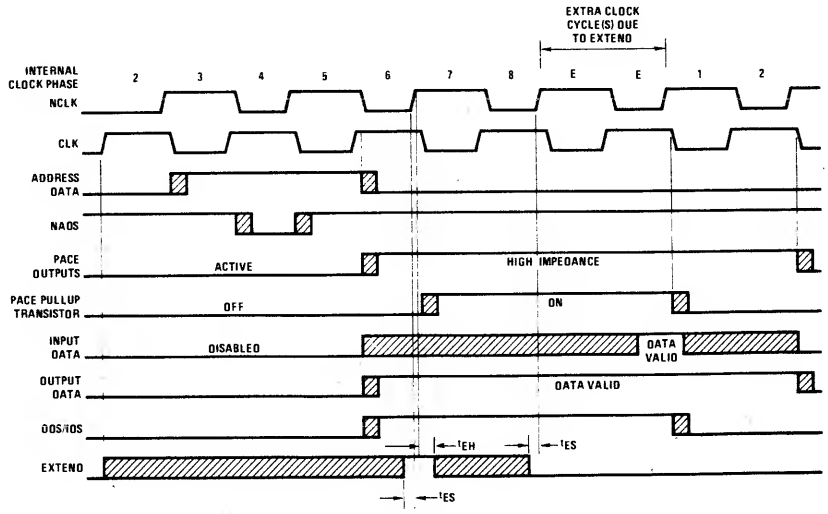


FIGURE 9. Extend I/O Signal Timing

absolute maximum ratings

All Input or Output Voltages with Respect to Most Positive Supply Voltage (V_{BB}) +0.3V to −21.5V

Operating Temperature Range 0°C to +70°C

Storage Temperature Range −65°C to +150°C

Lead Temperature (Soldering, 10 seconds) 300°C

electrical characteristics (T_A = 0°C to +70°C, V_{SS} = +5V ±5%, V_{GG} = −12V ±5%, V_{BB} = V_{SS} + 3V ±0.5V)

PARAMETER	CONDITIONS	MIN	MAX	UNITS
OUTPUT SPECIFICATIONS				
D00–D15, F11–F14, ODS, IDS, NADS (These are open drain outputs which may be used to drive DS3608 sense amplifiers, or may be used with pull-down resistors to provide a voltage output.)				
Logic "1" Output Current (Except F11–F14)	V_{OUT} = 2.4V	−1.0	−5.0	mA
Logic "1" Output Current, F11–F14 (Note 7)	V_{OUT} = 2.4V	−0.7	−5.0	mA
Logic "0" Output Current	$V_{GG} \leqslant V_{OUT} \leqslant V_{SS}$		±10	μA
NHALT, CONTIN (Low Power TTL Output.)				
Logic "1" Output Voltage	I_{OUT} = −650μA	2.4		V
Logic "0" Output Voltage	I_{OUT} = 300μA		0.4	V
INPUT SPECIFICATIONS				
D00–D15, NIR2–NIR5, EXTEND, JC13–JC15, CONTIN, NINIT, NHALT (These are TTL compatible inputs.) (Note 2)				
Logic "1" Input Voltage		V_{SS}−1	V_{SS}+0.3	V
Logic "0" Input Voltage		V_{SS}−7	V_{SS}−4	V
Pullup Transistor "ON" Resistance (D00–D15) (Note 3)	V_{IN} = V_{SS}−1V		7	kΩ
Pullup Transistor "ON" Resistance (all others)	V_{IN} = V_{SS}−1V		5	kΩ
Logic "0" Input Current (D00–D15)	V_{IN} = 0.4		−1.8	mA
Logic "0" Input Current (NHALT, CONTIN)	V_{IN} = 0.4		−12	mA
Logic "0" Input Current (all others)	V_{IN} = 0.4		−3.6	mA
Capacitance, Input and Output (except clocks)	V_{IN} = V_{SS}, f_T = 500 kHz		20	pF
BPS (This is a MOS Level Input.) (Note 4)				
Logic "1" Input Voltage		V_{SS}−1	V_{SS}+0.3	V
Logic "0" Input Voltage		V_{GG}	V_{SS}−7	V
Logic "1" Input Current	V_{IN} = V_{SS}−1V		100	μA
CLK, NCLK (These are MOS Clock Inputs)				
Clock "1" Voltage (Note 5)		V_{SS}−1	V_{SS}+0.3	V
Clock "0" Voltage		V_{GG}	V_{GG}+1	V
Input Capacitance (Note 6)		30	150	pF
Bias Supply Current	V_{BB} = V_{SS} +3.0V		100	μA
V_{GG} Supply Current	t_p = .65μs, T_A = 25°C		40	mA
V_{SS} Supply Current	t_p = .65μs, T_A = 25°C		85	mA

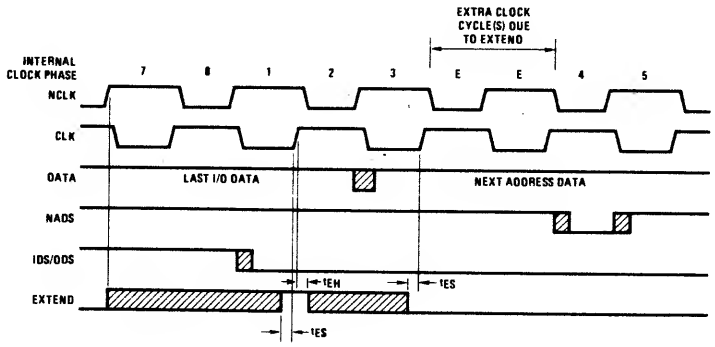


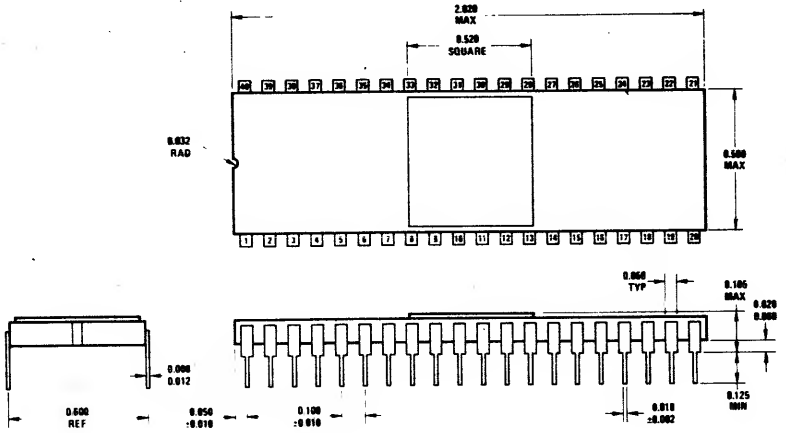
FIGURE 10. Suspend I/O Signal Timing

TIMING SPECIFICATIONS (See *Figures 5 to 10* for additional timing information.)

CLK, NCLK (See *Figure 5*) (Referenced to 10% and 90% Amplitude)				
Rise and Fall Time (t_r, t_f)		10	50	ns
Clock Width ($t_{W\ CLK}$, $t_{W\ NCLK}$)		300	375	ns
Clock Non-Overlap (t_{NOVA}, t_{NOVB})		5		ns
Clock Period (t_p)		.65	.8	μs
EXTEND				
Individual Extend Duration			2	μs
Extend Setup Time (t_{ES}) (Note 10)		100		ns
Extend Hold Time (t_{EH}) (Note 13)		20		ns
Propagation Delay (t_{DD})				
NHALT, CONTIN (Note 9)	C_L = 20 pF		200	ns
NADS, IDS, ODS, D00–D15 (Note 8)	V_{OUT} = 2.4V		100	ns
D00–D15				
Input Setup Time (t_{DS}) (Note 11)		200		ns
Hold Time (t_{DH}) (Note 12)		0		ns
Turn-on or Turn-off Time of Pullup Transistor (t_{DC}) (Note 13)		150		ns
F11–F14 Pulse Flag (PFLG) Pulse Width		$4t_p$ –300	$4t_p$ +300	ns
NINIT Initialization Pulse Width		8		clock periods
NIR2–NIR5 Input Pulse Width to Set Latch		1		clock periods

Note 1: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under dc electrical characteristics.
Note 2: Pullup transistor provided on chip (See *Figure 4*.)
Note 3: Pullup transistors on JC13, JC14, JC15 are turned on one out of 8 clock intervals. Pullup transistors on D00–D15 are turned on during last clock period of Input Data Strobe (IDS). Other pullup transistors are on continuously when in data input mode.
Note 4: Pulldown transistor provided on chip.
Note 5: Clamp diodes and series damping resistors may be required to prevent clock overshoot.
Note 6: Capacitance is not constant and varies with clock voltage and internal state of processor.
Note 7: For $V_{SS} \geq V_{OUT} \geq 2.0V$ output current is a linear function of V_{OUT}.
Note 8: Delay measured from valid logic level on clock edge initiating change to valid current output level
Note 9: Delay measured from valid logic level on clock edge initiating change to valid voltage output level.
Note 10: With respect to rising edge of NCLK. (See *Figure 9* and *10*.)
Note 11: With respect to falling edge of CLK. (See *Figure 7*.)
Note 12: With respect to the valid "0" level on the falling edge of Input Data Strobe (IDS). (See *Figure 7*.)
Note 13: With respect to valid logic level of appropriate clock.

physical dimensions



Cavity Dual-In-Line Package (D)
Order Number IPC-16A/520D

Manufactured under one or more of the following U.S. patents: 3083262, 3189758, 3231797, 3303356, 3317671, 3323071, 3381071, 3408542, 3421025, 3426423, 3440498, 3518750, 3519897, 3557431, 3560765, 3566218, 3571630, 3575609, 3579059, 3593069, 3597640, 3607469, 3617859, 3631312, 3633052, 3638131, 3648071, 3651565, 3693248.

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